WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a substrate having a semiconductor region,

a first insulating film formed on said semiconductor region and having a property of reflowing due to a heat treatment under predetermined conditions,

a second insulating film formed on said first insulating film and containing at least silicon nitride, and

a supporting film formed on at least one of the upper and lower surfaces of said second insulating film for applying to said second insulating film a stress against deformation of said second insulating film caused by said heat treatment.

2. A semiconductor device as set forth in Claim 1, further including a third insulating film formed at a higher level than said first insulating film and having a property of reflowing due to a heat treatment under said predetermined conditions.

3. A semiconductor device as set forth in Claim 1, wherein said supporting film is patterned so as to cover at least a region including a formation region of said second insulating film with respect to a common projection plane.

4. A semiconductor device as set forth in Claim 1, wherein

said semiconductor device is a stacked DRAM cell comprising a gate formed on said semiconductor region, an impurity diffusion layer formed in a region sideways of said gate in said semiconductor region, an interlayer insulating film formed on said gate and said semiconductor region, a storage node filling an opening formed in said interlayer insulating film and extending over a part of said interlayer insulating film, a capacitor insulating film formed for coverage over said storage node and said interlayer insulating film, and a plate electrode formed in opposed relation with said storage node via said capacitor insulating film,

said first insulating film defining said interlayer insulating film,

said second insulating film defining said capacitor insulating film,

said supporting film comprising an insulating film interposed between said interlayer insulating film and said capacitor insulating film.

5. A semiconductor device as set forth in Claim 1, wherein said semiconductor device is a stacked DRAM cell comprising a gate formed on said semiconductor region, an impurity diffusion layer formed in a region sideways of said gate in said semiconductor region, an interlayer insulating film formed on said gate and said semiconductor region, a storage

node filling an opening formed in said interlayer insulating film and extending over a part of said interlayer insulating film, a capacitor insulating film formed for coverage over said storage node and said interlayer insulating film, and a plate electrode formed in opposed relation with said storage node via said capacitor insulating film,

said first insulating film defining said interlayer insulating film,

said second insulating film defining said capacitor insulating film,

said supporting film defining said plate electrode.

6. A semiconductor device as set forth in Claim 4, wherein said storage node is a cylindrical storage node, and

wherein an etching stopper film is further provided as overlying said supporting film and underlying said storage node and capacitor insulating film so as to be utilized during the formation of the cylindrical storage node.

7. A semiconductor device as set forth in Claim 1, wherein said second insulating film comprises a silicon nitride film.

8. A semiconductor device as set forth in Claim 1, wherein said semiconductor device is a stacked DRAM cell comprising

a gate formed on said semiconductor region, an impurity diffusion layer formed in a region sideways of said gate in said semiconductor region, an interlayer insulating film formed on said gate and said semiconductor region, a storage node filling an opening formed in said interlayer insulating film and extending over a part of said interlayer insulating film, a capacitor insulating film formed for coverage over said storage node and said interlayer insulating film, and a plate electrode formed in opposed relation with said storage node via said capacitor insulating film,

said first insulating film defining said interlayer insulating film,

said second insulating film defining said capacitor insulating film and comprising an oxidized silicon nitride film formed by oxidizing a silicon nitride film,

said supporting film defining said plate electrode and covering a region including a formation region of said capacitor insulating film with respect to a common projection plane,

said interlayer insulating film having a property of not reflowing due to a heat treatment for oxidizing said silicon nitride film.

9. A semiconductor device as set forth in Claim 6, wherein a lower surface of a cylindrical portion of said

cylindrical storage node is spaced from a top surface of said etching stopper film, and

wherein said capacitor insulating film is formed for coverage over surfaces of said cylindrical storage node and said etching stopper film.

10. A semiconductor device as set forth in Claim 6, wherein said etching stopper film comprises a silicon nitride film.

11. A semiconductor device as set forth in Claim 3,

wherein said storage node is a cylindrical storage node, and

wherein said supporting film comprises a TEOS film and serves as an etching stopper film during the formation of the cylindrical storage node.

12. A semiconductor device as set forth in Claim 1, wherein said first insulating film comprises a BPSG film.

13. A semiconductor device as set forth in Claim 1, wherein said supporting film comprises a silicon oxide film.

14. A process for fabrication of a semiconductor device comprising the steps of:

a first step to deposit a first insulating film on a semiconductor substrate, the first insulating film having a

property of reflowing due to a heat treatment under predetermined conditions;

a second step to perform a first heat treatment under said predetermined conditions thereby causing said first insulating film to reflow for planarization thereof;

a third step to lay a second insulating film containing silicon nitride over said first insulating film;

a fourth step conducted after said second step and prior to or subsequent to said third step so as to form a supporting film on the substrate, the supporting film having a property of not reflowing due to a heat treatment under said predetermined conditions;

a fifth step following said fourth step so as to deposit a third insulating film on the substrate, the third insulating film having a property of reflowing due to a heat treatment under said predetermined conditions; and

a sixth step to perform a second heat treatment under said predetermined conditions thereby causing said third insulating film to reflow for planarization thereof,

wherein in said sixth step, a stress against deformation of said second insulating film is applied thereto by said supporting film.

15. A process for fabrication of a semiconductor device as set forth in Claim 14, further including a step conducted after said third and fourth steps and prior to said fifth step so as to pattern said second insulating film and said supporting film in a manner that said supporting film covers at least a region including a formation region of said second insulating film with respect to a common projection plane.

16. A process for fabrication of a semiconductor device as set forth in Claim 14,

wherein said fourth step is conducted prior to said third step,

further including a step following said third step so as to perform a third heat treatment under said predetermined conditions thereby oxidizing a surface of said second insulating film for formation of an oxidized silicon nitride film,

wherein in said step to perform the third heat treatment, a stress against deformation of said second insulating film is applied thereto by said supporting film.

17. A process for fabrication of a semiconductor device functioning as a stacked DRAM cell comprising the steps of:

a first step to deposit a first insulating film on a semiconductor substrate having an impurity diffusion layer,

the first insulating film having a property of reflowing due to a heat treatment under predetermined conditions;

a second step to perform a first heat treatment under said predetermined conditions thereby causing said first insulating film to reflow for planarization thereof;

a third step following said second step so as to form a supporting film having a property of not reflowing due to a heat treatment under said predetermined conditions;

a fourth step to form a contact hole extending through said supporting film and said first insulating film and to said impurity diffusion layer;

a fifth step to deposit a first conductive film for storage node on the substrate including said contact hole;

a sixth step to pattern said first conductive film for storage node for forming a storage node connected to said impurity diffusion layer;

a seventh step following said sixth step so as to deposit a second insulating film comprising a silicon nitride film for coverage over a surface of said storage node and an exposed surface of said supporting film;

an eighth step following said seventh step so as to perform a second heat treatment under said predetermined

conditions thereby oxidizing a surface of said second insulating film for formation of a capacitor insulating film comprising an oxidized silicon nitride film; and

a ninth step following said eighth step so as to form a conductive film for plate electrode on the substrate;

wherein in said eighth step, a stress against deformation of said second insulating film caused by said second heat treatment is applied thereto by said supporting film.

18. A process for fabrication of a semiconductor device as set forth in Claim 17, further including:

a step following said ninth step so as to form a third insulating film on the substrate, the third insulating film having a property of reflowing due to a heat treatment under said predetermined conditions; and

a step following the above step so as to perform a third heat treatment under said predetermined conditions thereby causing said third insulating film to reflow for planarization thereof;

wherein in said planarization step, a stress against deformation of said second insulating film caused by said third heat treatment is applied thereto by said supporting film.

19. A process for fabrication of a semiconductor device as

set forth in Claim 17,

wherein in said third step, the supporting film is formed of a TEOS film;

said process further including a step conducted after said fifth step and prior to said sixth step so as to form a core of cylindrical storage node on said first conductive film for storage node, the core comprising a BPSG film; and

a step following the above step so as to form a second conductive film for storage node on the substrate including said core of cylindrical storage node;

wherein in said sixth step, said first and second conductive films for storage node are patterned for forming a cylindrical storage node comprised of said first and second conductive films for storage node;

said process still further including a step conducted after said sixth step and prior to said seventh step so as to remove by etching said core of the cylindrical storage node;

wherein said supporting film serves as an etching stopper film in said sixth step and said step to remove the core of the cylindrical storage node.

20. A process for fabrication of a semiconductor device as set forth in Claim 19, further including a step conducted after

said third step and prior to said fourth step so as to form a film for gap production on said supporting film;

said fourth step wherein said contact hole is so formed as to extend through said film for gap production, as well;

said step to remove the core of the cylindrical storage node wherein said film for gap production is also removed thereby exposing a surface of said cylindrical storage node that contacts said film for gap production;

said seventh step wherein said second insulating film is deposited for coverage over the exposed surfaces of said cylindrical storage node and said supporting film.

21. A process for fabrication of a semiconductor device as set forth in Claim 17, further including a step conducted after said second step and prior to said third step so as to deposit on the substrate an insulating film for edge retention having a high etching selectivity to said first insulating film;

wherein in said third step, said contact hole is so formed as to extend through said insulating film for edge retention, as well.

22. A process for fabrication of a semiconductor device functioning as a stacked DRAM cell comprising the steps of:

a first step to deposit a first insulating film on a

substrate having an impurity diffusion layer, the first insulating film having a property of reflowing due to a heat treatment under predetermined conditions;

a second step to perform a first heat treatment under said predetermined conditions thereby causing said first insulating film to reflow for planarization thereof;

a third step following said second step so as to form a supporting film having a property of not reflowing due to a heat treatment under said predetermined conditions;

a fourth step to lay over said supporting film an etching stopper film utilized during a formation of a cylindrical storage node;

a fifth step to form a contact hole extending through said etching stopper film, supporting film and first insulating film and to said impurity diffusion layer;

a sixth step to deposit a first conductive film for storage node on the substrate including said contact hole;

a seventh step following said sixth step so as to form a core of cylindrical storage node on said first conductive film for storage node;

an eighth step following said seventh step so as to form a second conductive film for storage node on the substrate

including said core of cylindrical storage node;

a ninth step to pattern said first and second conductive films for storage node for forming a cylindrical storage node comprised of said first and second conductive films for storage node;

a tenth step following said ninth step so as to remove by etching said core of the cylindrical storage node;

an eleventh step following said tenth step so as to deposit a second insulating film comprising a silicon nitride film for coverage over a surface of said cylindrical storage node and an exposed surface of said supporting film;

a twelfth step following said eleventh step so as to perform a second heat treatment under said predetermined conditions thereby oxidizing a surface of said second insulating film for forming a capacitor insulating film comprising an oxidized silicon nitride film; and

a thirteenth step following said twelfth step so as to form a conductive film for plate electrode on the substrate;

wherein in said twelfth step, a stress against deformation of said second insulating film and said etching stopper film caused by said second heat treatment is applied thereto by said supporting film.

23. A process for fabrication of a semiconductor device as set forth in Claim 22, further including a step following said thirteenth step so as to form on the substrate a third insulating film having a property of reflowing due to a heat treatment under said predetermined conditions; and

a step following the above step so as to perform a third heat treatment under said predetermined conditions thereby causing said third insulating film to reflow for planarization thereof;

wherein in said planarization step for the third insulating film, a stress against deformation of said second insulating film and said etching stopper film caused by said third heat treatment is applied thereto by said supporting film.

24. A process for fabrication of a semiconductor as set forth in Claim 22, further including a step to form a film for gap production on said etching stopper film;

said fifth step wherein said contact hole is so formed as to extend through said film for gap production, as well;

said step for removal of said core of the cylindrical storage node wherein said film for gap production is also removed thereby to expose a surface of said cylindrical storage node that contacts said film for gap production;

wherein in said eleventh step, said second film is

deposited for coverage over the exposed surfaces of said cylindrical storage node and said supporting film.

25. A process for fabrication of a semiconductor device as set forth in Claim 22, further including a step conducted after said second step and prior to said third step so as to deposit on the substrate an insulating film for edge retention having a high etching selectivity to said first insulating film;

wherein in said fifth step, said contact hole is so formed as to extend through said insulating film for edge retention, as well.

26. A process for fabrication of a semiconductor device comprising the steps of:

a first step to deposit a first insulating film on a substrate having an impurity diffusion layer, the first insulating film having a property of reflowing due to a heat treatment under predetermined conditions;

a second step to perform a first heat treatment under said predetermined conditions thereby causing said first insulating film to reflow for planarization thereof;

a third step following said second step so as to deposit a second insulating film comprising a silicon nitride film on the substrate; and

a fourth step following said third step so as to perform a second heat treatment under such conditions as not to cause said first insulating film to reflow thereby oxidizing a surface of said second insulating film for forming a capacitor insulating film comprising an oxidized silicon nitride film.

27. A process for fabrication of a semiconductor device as set forth in Claim 26, wherein said first step comprises depositing the first insulating film comprising a BPSG film having a reflow temperature of not less than 830°C; and

wherein said fourth step comprises thermal oxidation performed at temperatures of not more than 820°C.

28. A process for fabrication of a semiconductor device as set forth in Claim 26, wherein in said first step the first insulating film comprising a BPSG film containing 2.0 to 6.0 wt% of phosphorus and 1.0 to 4.0 wt% of boron is deposited.

29. A process for fabrication of a semiconductor device as set forth in Claim 26, wherein said fourth step comprises thermal oxidation process performed in a dry atmosphere.

30. A process for fabrication of a semiconductor device as set forth in Claim 26, further including a step conducted prior to said third step so as to nitride exposed surfaces of said storage node and said first insulating film.

31. A process for fabrication of a semiconductor device as

set forth in Claim 30, wherein said nitriding step comprises heat treatment performed in an atmosphere of nitrogen or ammonia.

32. A process for fabrication of a semiconductor device as set forth in Claim 26, further including steps conducted between said second and third steps,

a step to form a contact hole extending through said first insulating film to said impurity diffusion layer;

a step to deposit a conductive film for storage node on the substrate including said contact hole; and

a step to pattern said conductive film for storage node for forming a storage node connected to said impurity diffusion layer;

wherein in said third step, said second insulating film is deposited on the substrate including a surface of said storage node; and

said process further including a step following said fourth step so as to form a conductive film for plate electrode on the substrate.

33. A process for fabrication of a semiconductor device as set forth in Claim 30, wherein a cylindrical storage node is formed as said storage node.

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